EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	22	L1 and ((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ("media access controller" MAC)) and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 18:38
L1	42690	(324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17 716/1,4-5,16-18).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 18:37
S54	51	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same "media access controller") and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 15:57
S53	31	S52 and debugger	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 15:38
S52	494	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ("media access controller" MAC)) and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 15:37
S51	36	S49 not S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:35
S50	9	S49 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:35
S49	45	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3 and ("media access controller" MAC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:34
S48	163	((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and ("media access controller" MAC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:34
S47	5	S46 not S45	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:07

S46	14	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and ("media access controller" MAC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 14:05
S45	9	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3 and ("media access controller" MAC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/09 13:59
S41	11	S40 and ((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select$3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:27
S44	0	S41 not S43	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:26
S43	11	S42 and ((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select$3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:26
S42	30892	(324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17 716/1,4-5,16-18).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:26
S40	30892	(324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17 716/1,4-5,16-18).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:24
S37	7	S36 and ((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select$3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:24
S36	28968	(324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17 716/1,4-5,16-18).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/17 16:24
S39	4	S36 and S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 15:20

S38	8	("6829751" "6211697" "6260087" "6531889").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 15:20
S31	8	("6829751" "6211697" "6260087" "6531889").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 15:20
S22	35	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) same ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 15:18
S15	2792	((ASIC or application adj specific adj integrated adj circuit or standard near cell or component or IC or integrated adj circuit) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic) same (debug$4 analyz$3 compar$3 emulat$3)) and (select$3 switch multiplex$3 MUX)) and (324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 15:17
S35	2	"6434735 ".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/17 10:31
S30	1	"20010125" and Bailis	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 14:13
S29	13754	"20010125"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 14:13
S1	46	("6260087" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 14:12
S27	11	S26 and (ASIC or "application specific integrated circuit" or "standard cell")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 13:45
S26	41	S25 not S22	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 13:44

S25	43	((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3) near (function client))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 13:44
S23	1290	((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 13:43
S24	1	((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) near5 (debug$4 analyz$3)) same ((manipultat$ alter$3 select$3) near3 ((bus internal) near signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 13:42
S12	402	((ASIC or application adj specific adj integrated adj circuit or standard adj cell) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) same (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 12:29
S10	7440	(ASIC or application adj specific adj integrated adj circuit or standard adj cell) and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) and (debug$4 analyz $3 correct improve fix repair) and (select$3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/14 12:29
S21	6	((US-6577158-$ or US-6460148-$ or US-6260087-$ or US-6247147-$ or US-6173419-$ or US-5867037-$ or US-5794033-$ or US-5687325-$ or US-6178541-$ or US-6181159-$).did. or (US-20030062922-$ or US-20020101260-$).did. or (GB-2289964-$).did.) and debug	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 14:42
S20	13	(US-6577158-$ or US-6460148-$ or US-6260087-$ or US-6247147-$ or US-6173419-$ or US-5867037-$ or US-5794033-$ or US-5687325-$ or US-6178541-$ or US-6181159-$).did. or (US-20030062922-$ or US-20020101260-$).did. or (GB-2289964-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/04/06 14:40
S19	625	((ASIC or application adj specific adj integrated adj circuit or standard adj cell or IC or integrated adj circuit) and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic)) same (debug$4 analyz$3 compar$3 emulat$3) and (select$3 switch multiplex$3 MUX)) and (324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 12:08
S17	2252	((ASIC or application adj specific adj integrated adj circuit or standard adj cell or IC or integrated adj circuit) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic) same (debug$4 analyz$3 compar$3 emulat$3)) and (select$3 switch multiplex$3 MUX)) and (324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 12:08

S18	2648	(ASIC or application adj specific adj integrated adj circuit or standard adj cell or IC or integrated adj circuit) and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic)) same (debug$4 analyz$3 compar$3 emulat$3) and (select$3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 12:07
S16	23124	(ASIC or application adj specific adj integrated adj circuit or standard adj cell or IC or integrated adj circuit) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic) same (debug$4 analyz$3 compar$3 emulat$3)) and (select$3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 12:03
S14	48327	(ASIC or application adj specific adj integrated adj circuit or standard near cell or component or IC or integrated adj circuit) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic) same (debug$4 analyz$3 compar$3 emulat$3)) and (select$3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 12:00
S13	82	(((ASIC or application adj specific adj integrated adj circuit or standard adj cell) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) same (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)) and receiv$3 and transmit$4 and interfac$3) and (324/73.1,210 326/39,41,37,38 365/230.03,189.02,189.03,230.02 395/702,704 702/117,118 709/224 710/100,104,131 714/28,30,39,718,724,725,734,742 716/12,17).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 11:59
S11	877	(ASIC or application adj specific adj integrated adj circuit or standard adj cell) and ((FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array) same (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 11:56
S8	16	(((("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)) and (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 10:04
S7	16	((("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)) and (debug$4 analyz$3 correct improve fix repair)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 10:04

S4	36	("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 10:04
S9	0	((((("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)) and (debug$4 analyz$3 correct improve fix repair)) not ((((("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)) and (debug$4 analyz$3 correct improve fix repair)) and (select $3 switch multiplex$3 MUX))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 10:03
S5	23	(("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 09:56
S6	1	((("6260087" "6173419" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)) not ((("6260087" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 09:50

S2	22	(("6260087" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)) and (ASIC or application adj specific adj integrated adj circuit or standard adj cell)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 09:49
S3	34	("6260087" "6247147" "6182247" "6181159" "6178541" "6230119" "6260182" "6134173" "6182206" "6191614" "6209118" "6211697" "6219819" "6223313" "6219833" "6223148" "6226776" "6237021" "6249143" "6252422" "6253267" "6256296" "6260185").pn. and (FPGA CLB PLA FPLA LAB ((programmable configurable) near2 logic) logic adj array)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/06 09:48

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